(12) UK Patent Application (19) GB (11) 2 151 874 A

(43) Application published 24 Jul 1985

(21) Application No 8429542

(22) Date of filing 22 Nov 1984

(30) Priority data

(31) 58/218711 (32) 22 Nov 1983 (33) JP

(71) Applicant
Canon Kabushiki Kaisha (Japan),
3-30-2 Shimomaruko, Ohta-ku, Tokyo, Japan

(72) Inventors
Katsumi Nakagawa,
Katsunori Hatanaka,
Shinichi Seitoh,
Yasuo Kuroda,
Toshiyuki Komatsu

(74) Agent and/or Address for Service
R. G. C. Jenkins & Co.,
12-15 Fetter Lane, London EC4A 1PL

(51) INT CL^4
H04N 3/14 G09G 3/20

(52) Domestic classification
H4F CC D30K D42E D42V D83B
G5C A310 A342 HB
H1K 11A3 11C1A 11D1 11D 1CA 1EA 1EB 4C11 4C14
9C3 GAX

(56) Documents cited
GB A 2096814

(58) Field of search
H4F
G5C

(54) Driving a matrix of thin-film light-sensitive or display elements

(57) A matrix comprising blocks, each made up of a set of thin-film unit elements of semiconductor, either light-sensitive or controlling a light valve, is driven by applying voltage pulses (T_1, T_2 etc) to the blocks in turn, and while each block is enabled, selected elements in that block are read or energized. To reduce dark current, a short pulse P is applied to all of the blocks in the gaps between the enabling pulses. The number of pulses P applied to each block before enablement may be finite, eg 5 to 10, and yet provide adequate reduction in dark current.

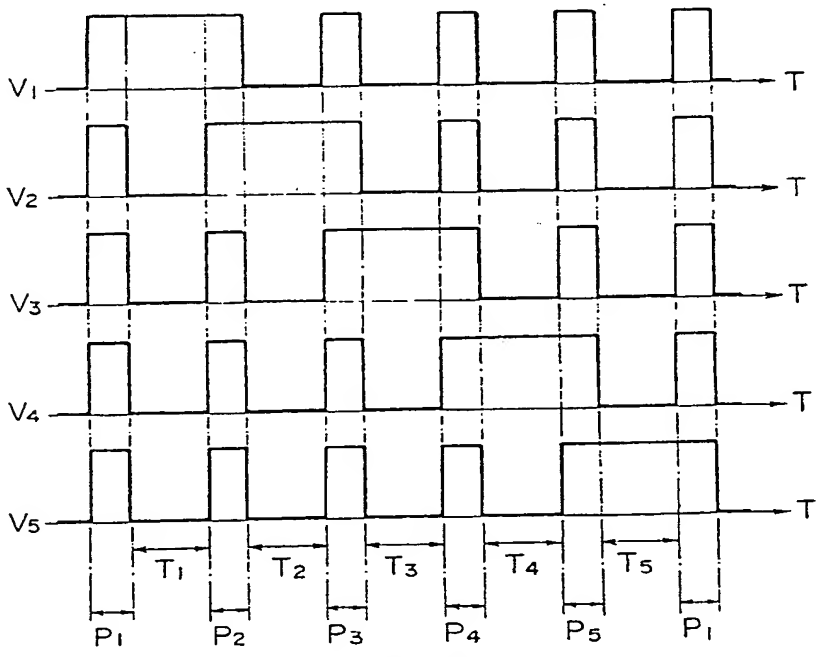


FIG. 7

GB 2 151 874 A

2151874

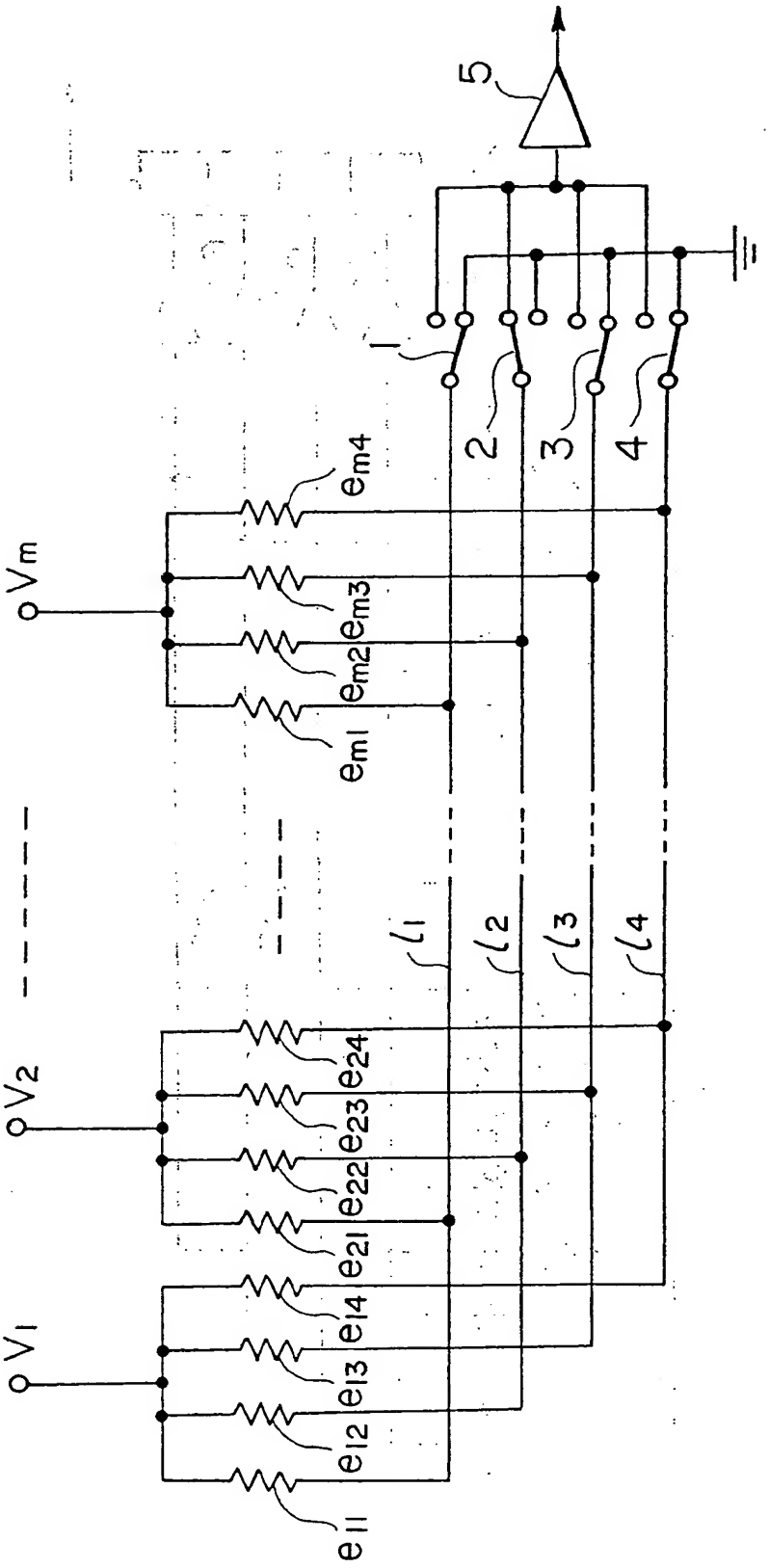


FIG. 1

2151874

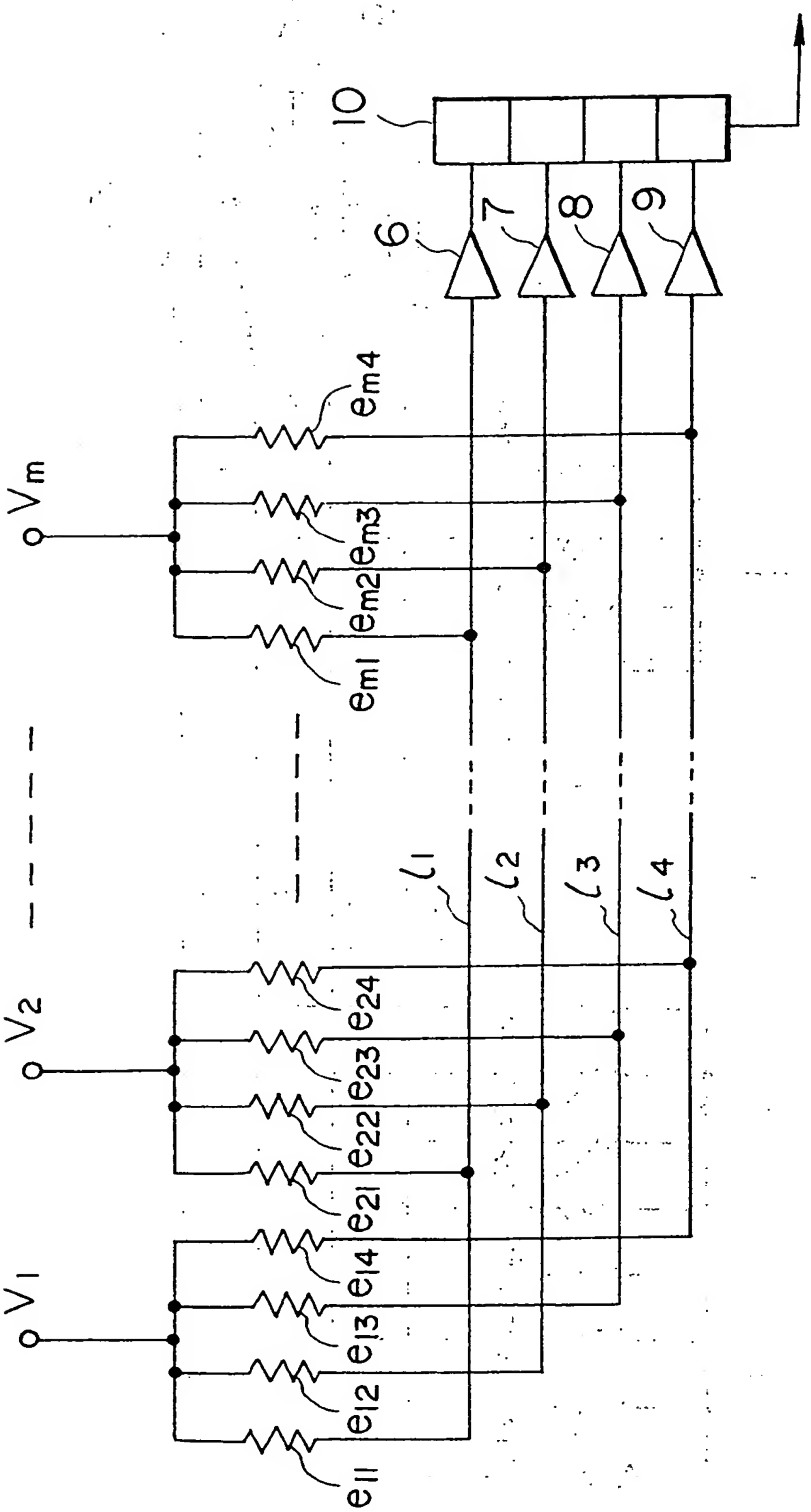


FIG. 2

2151874

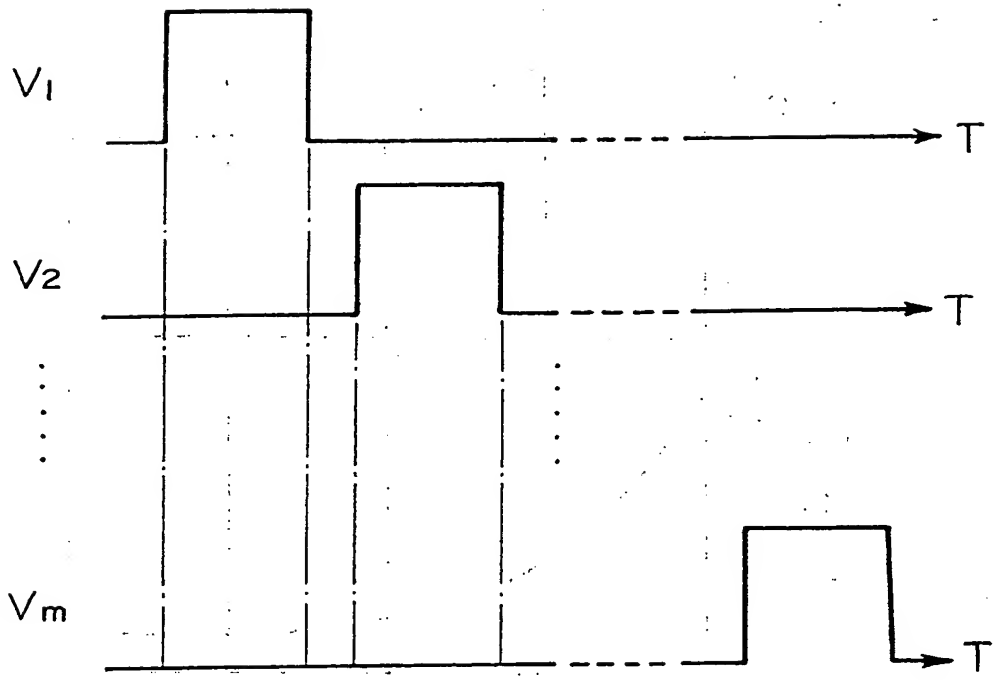


FIG. 3

2151874

FIG. 4A

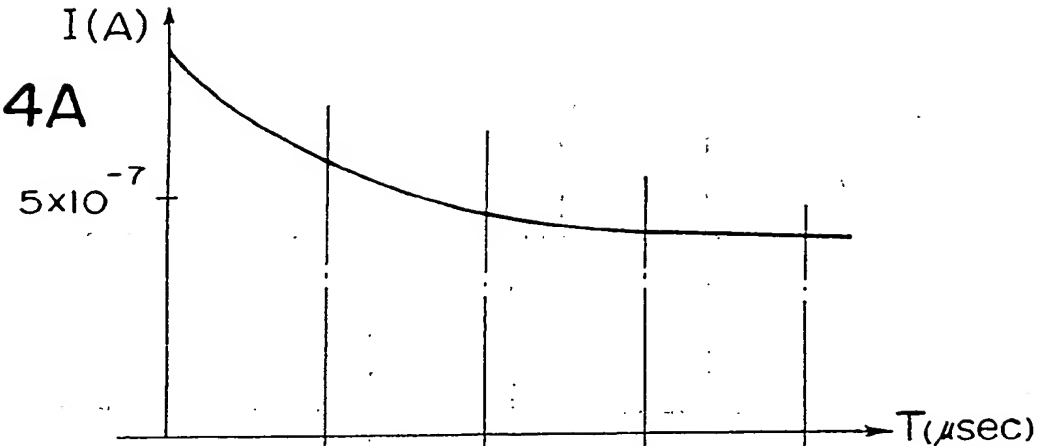


FIG. 4B

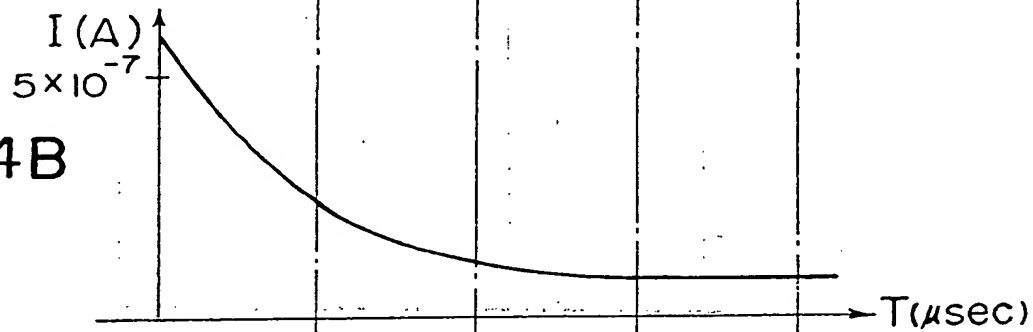
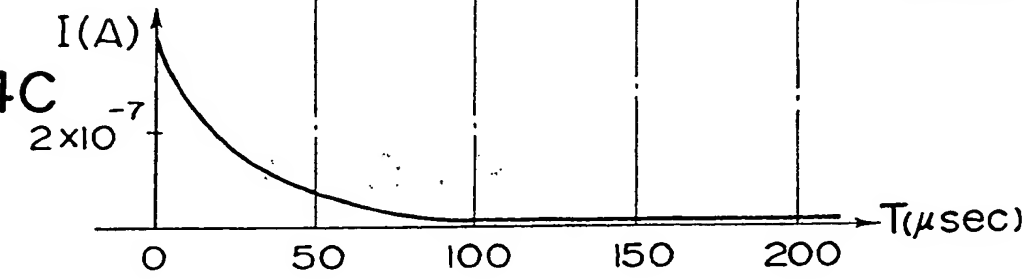


FIG. 4C



2151874

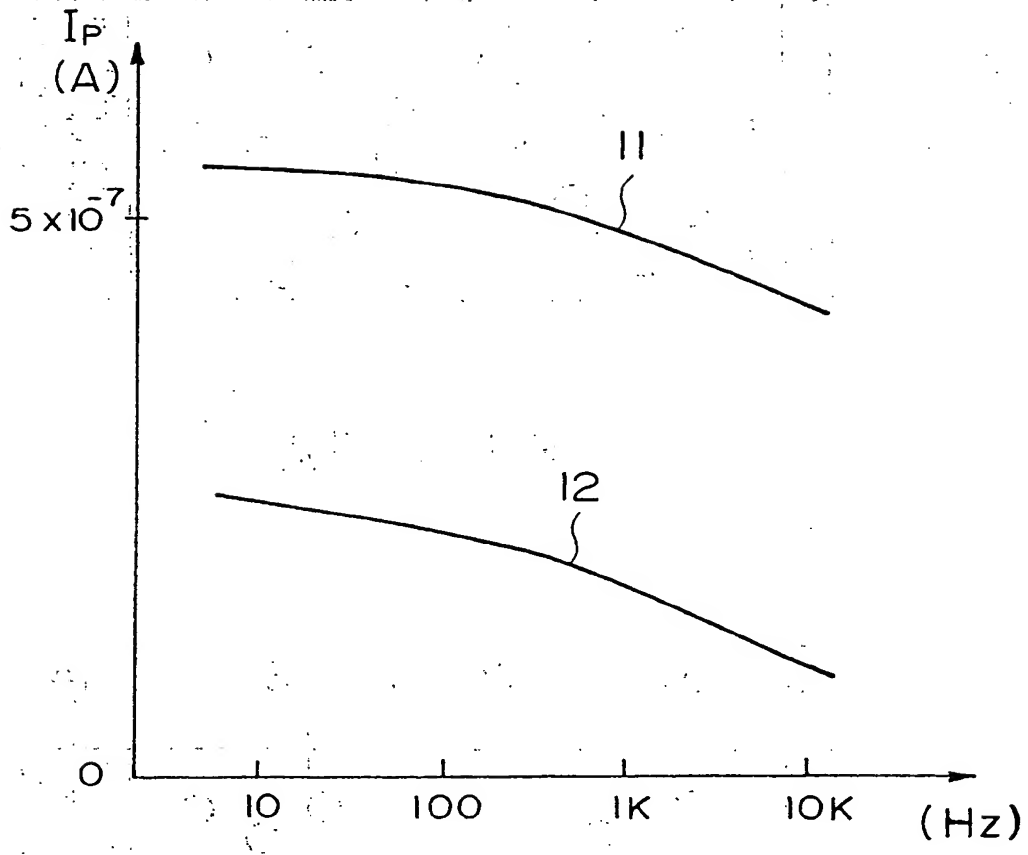


FIG. 5

WSDOCID <GB 2151874A 1>

2151874

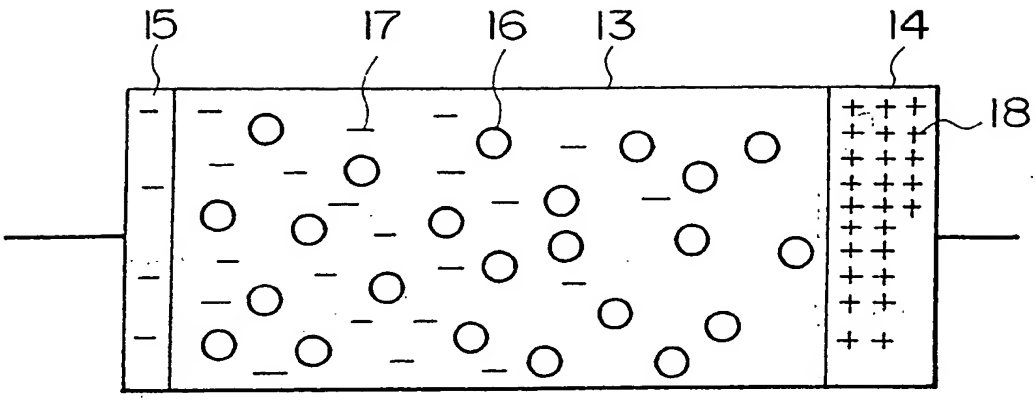


FIG. 6A

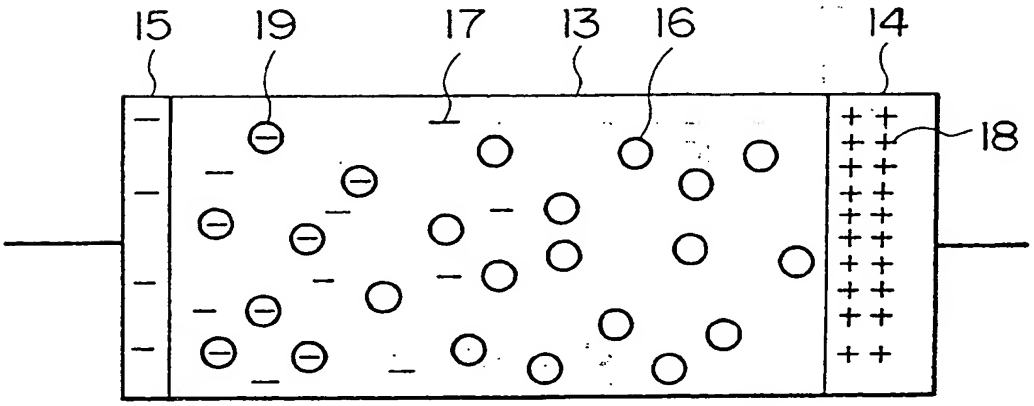


FIG. 6B

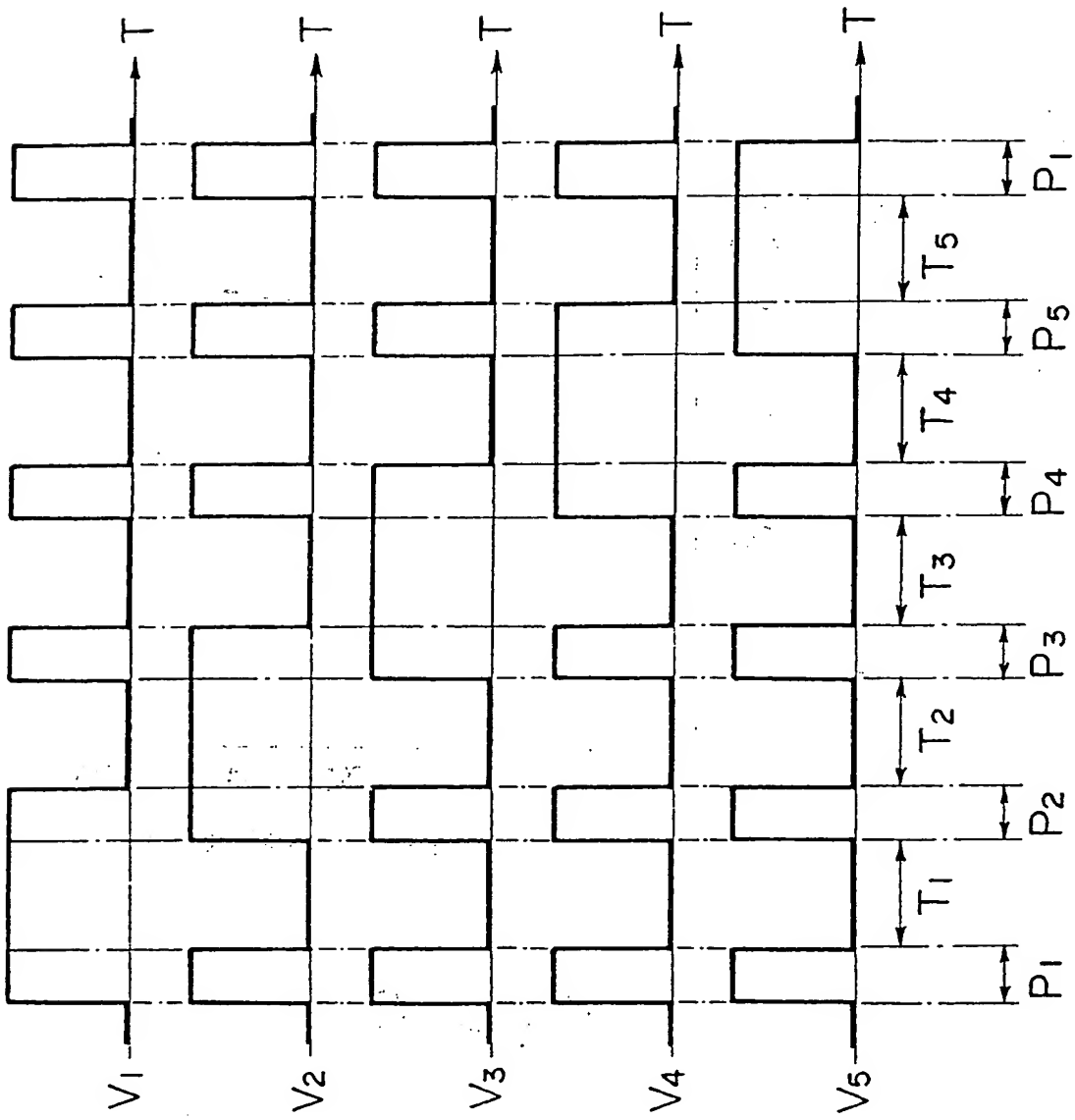


FIG. 7

2151874

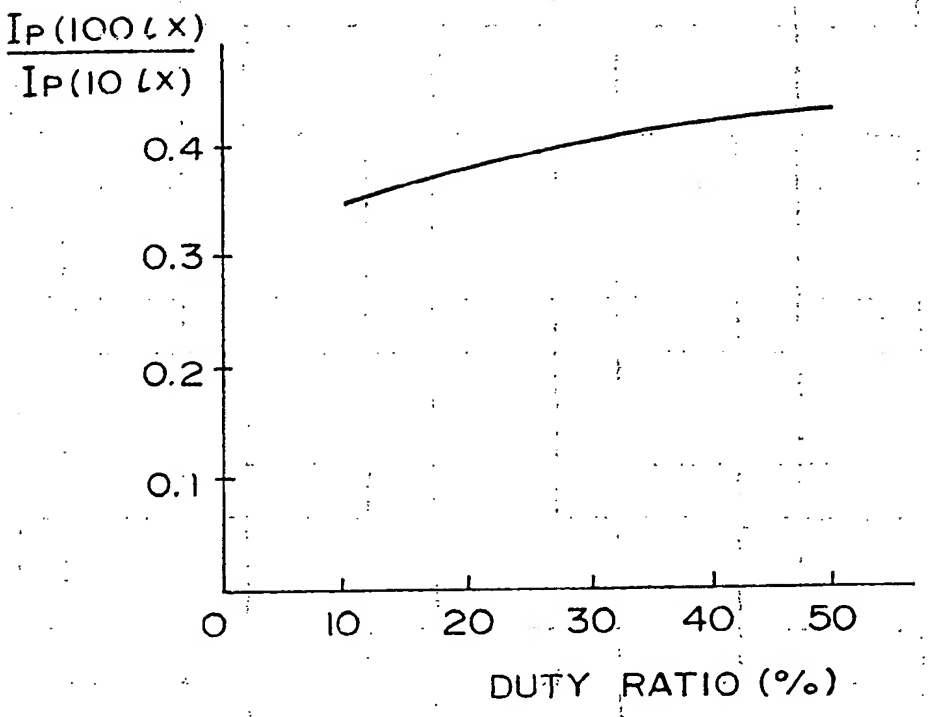


FIG. 8

2151874

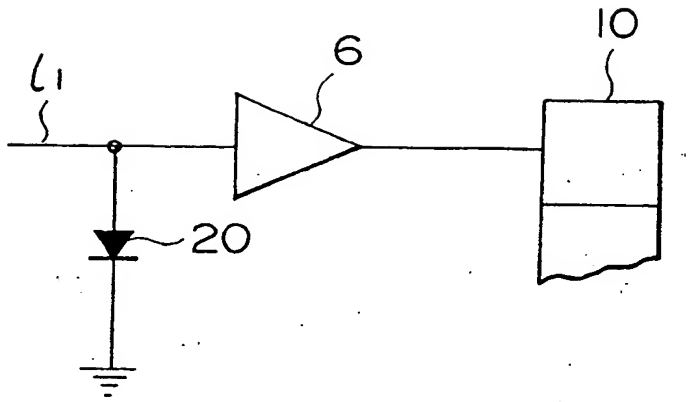


FIG. 9

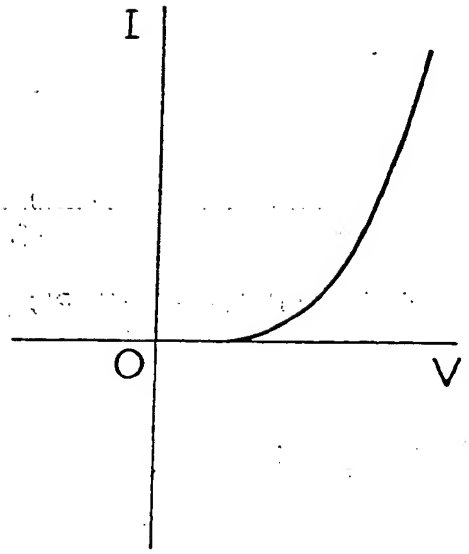


FIG. 10

2151874

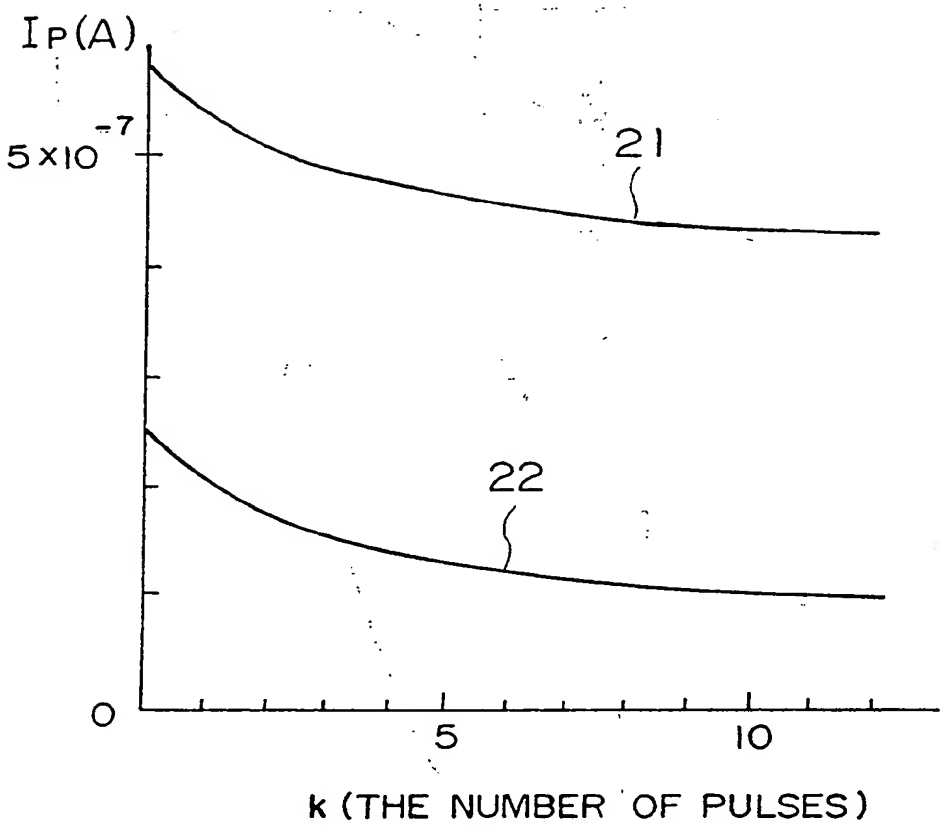


FIG. 11

2151874

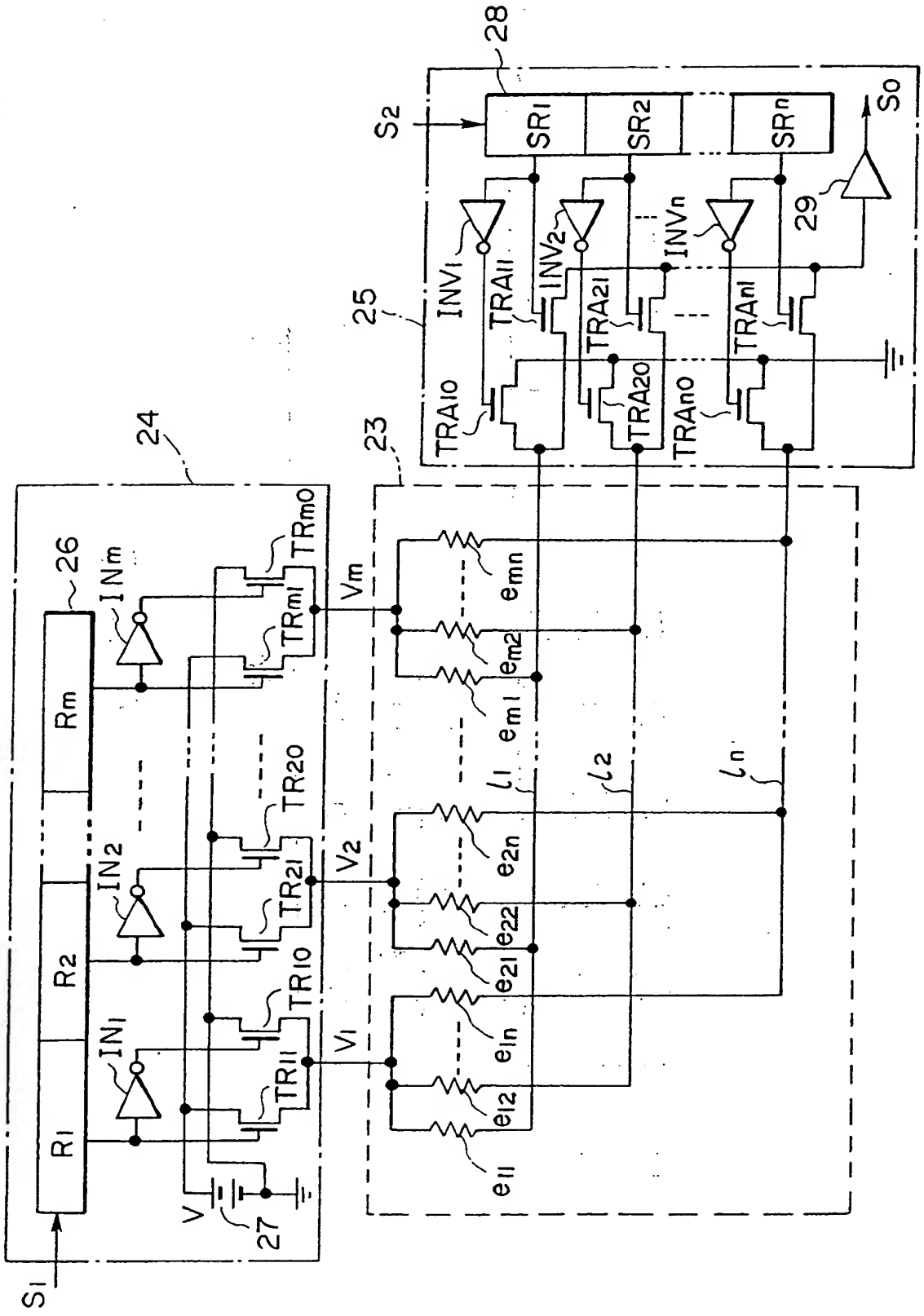


FIG. 12

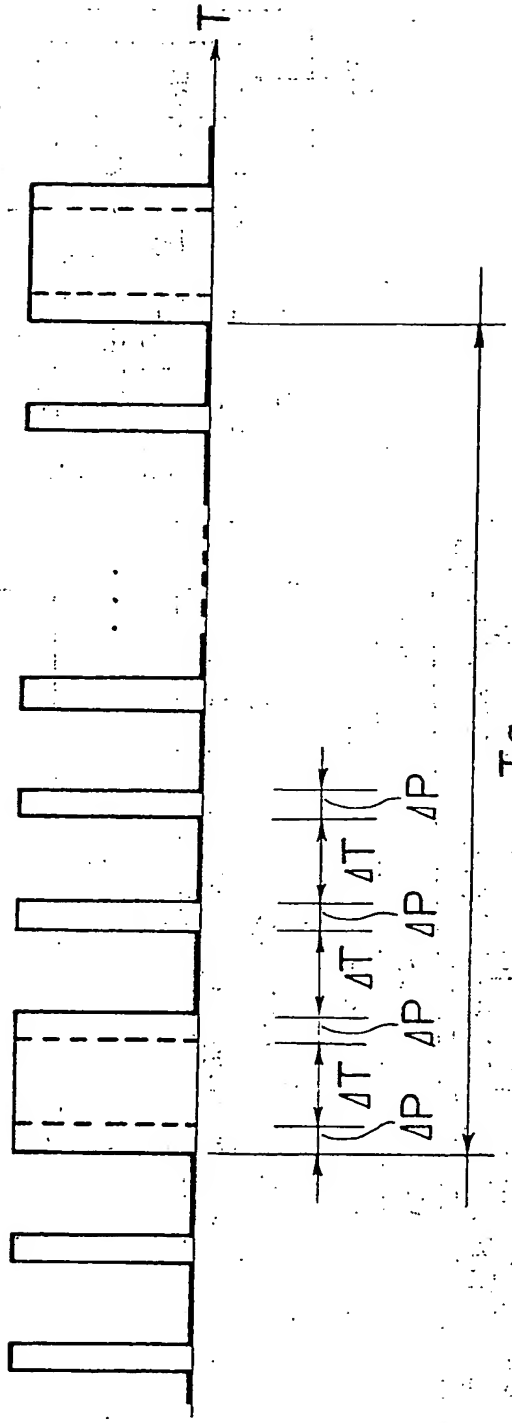


FIG. 13

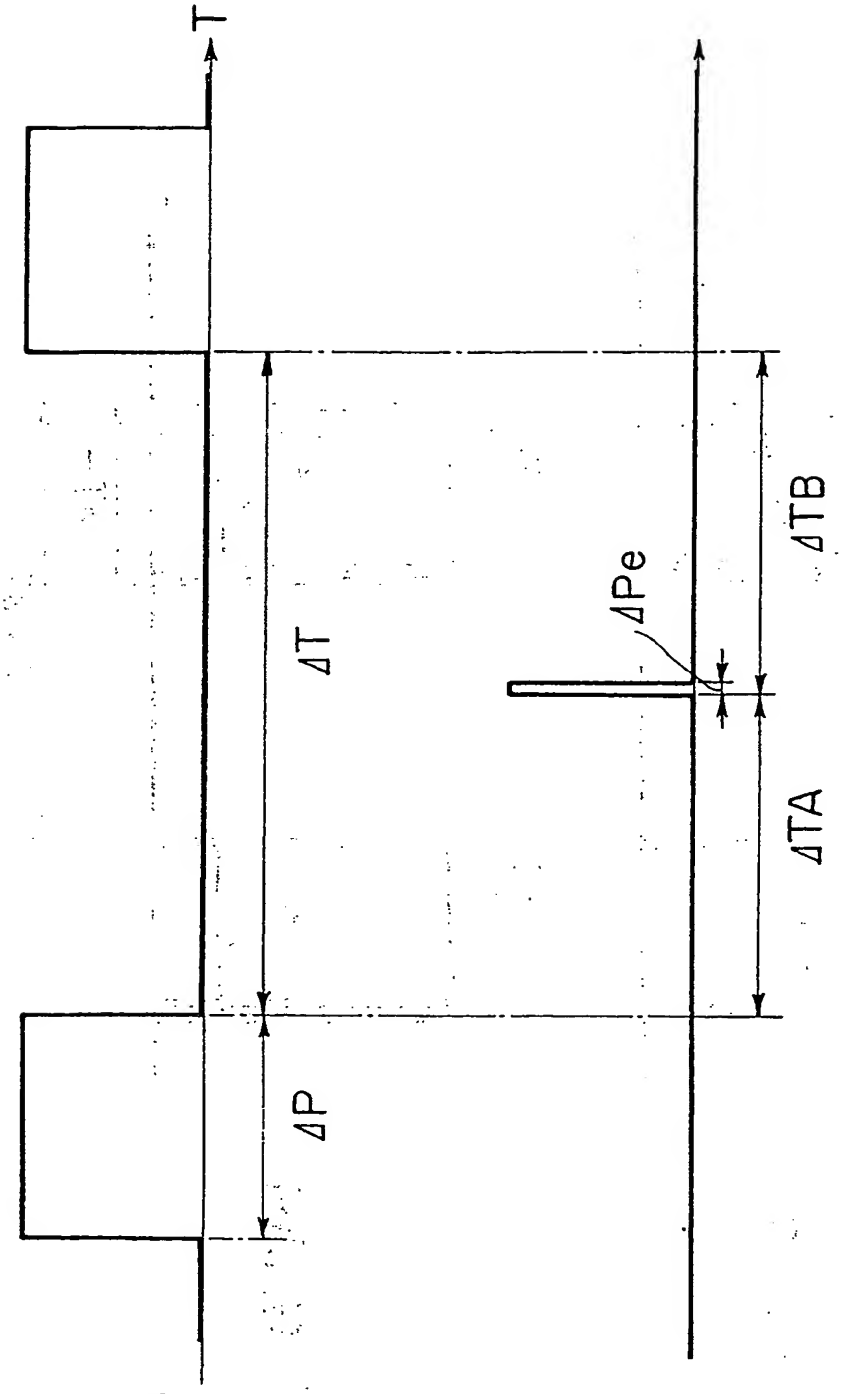


FIG. 14A

FIG. 14B

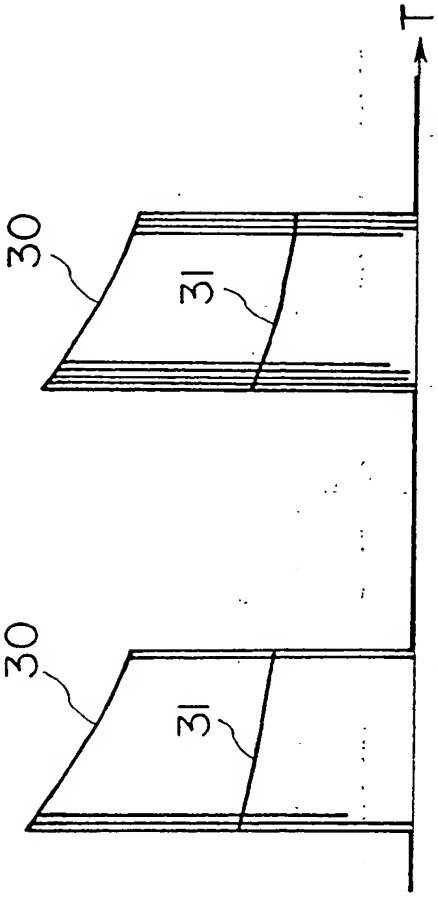


FIG. 15A

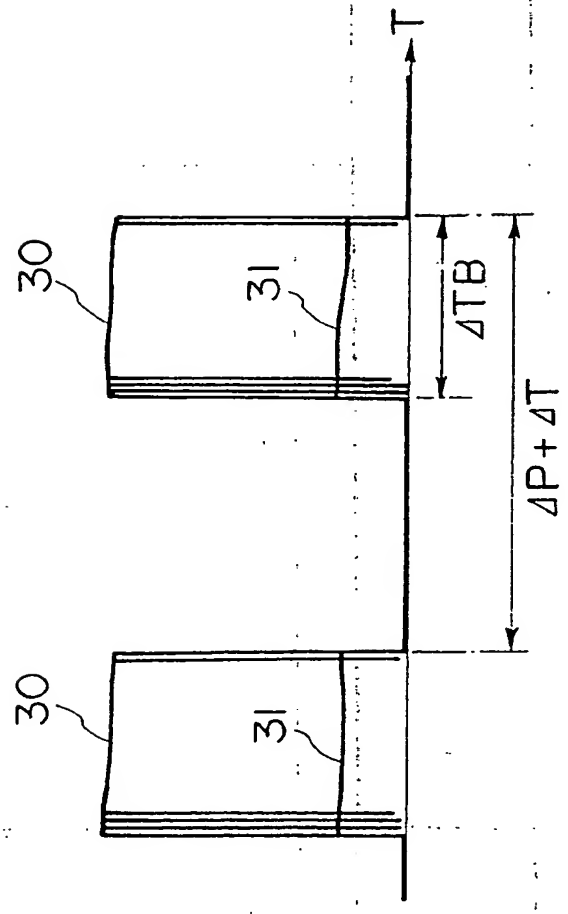


FIG. 15B

2151874

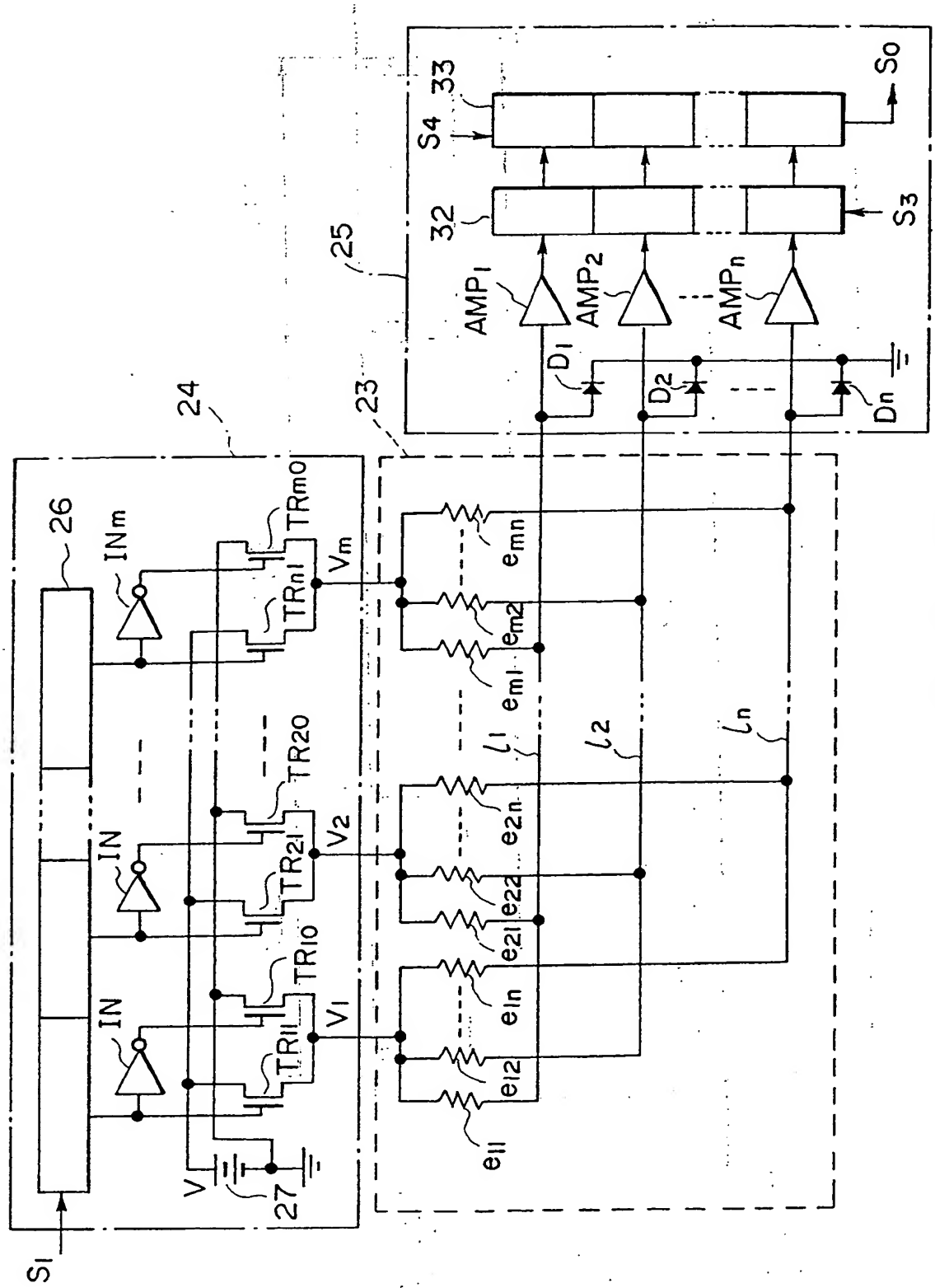


FIG. 16

2151874

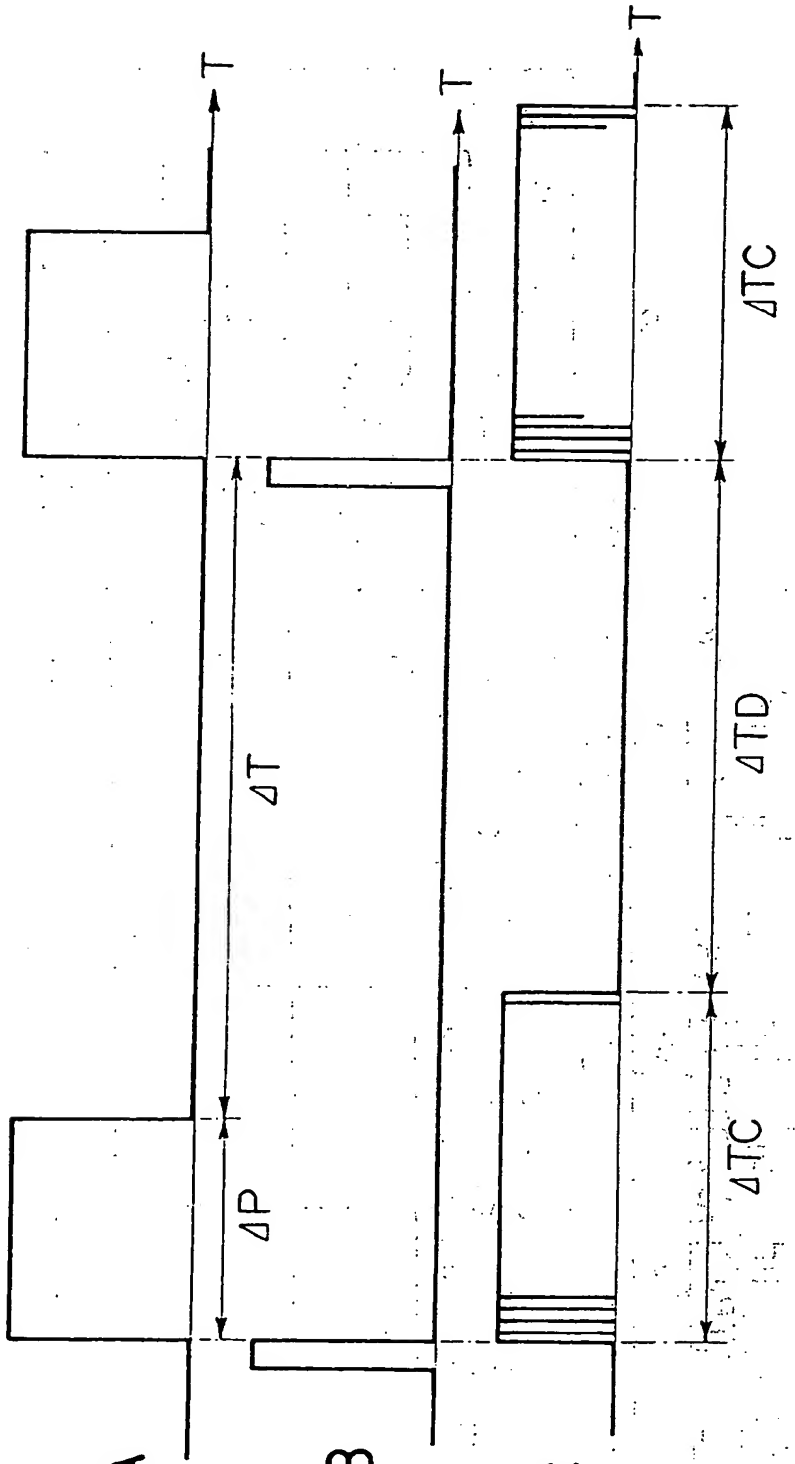


FIG.17A FIG.17B FIG.17C

2151874

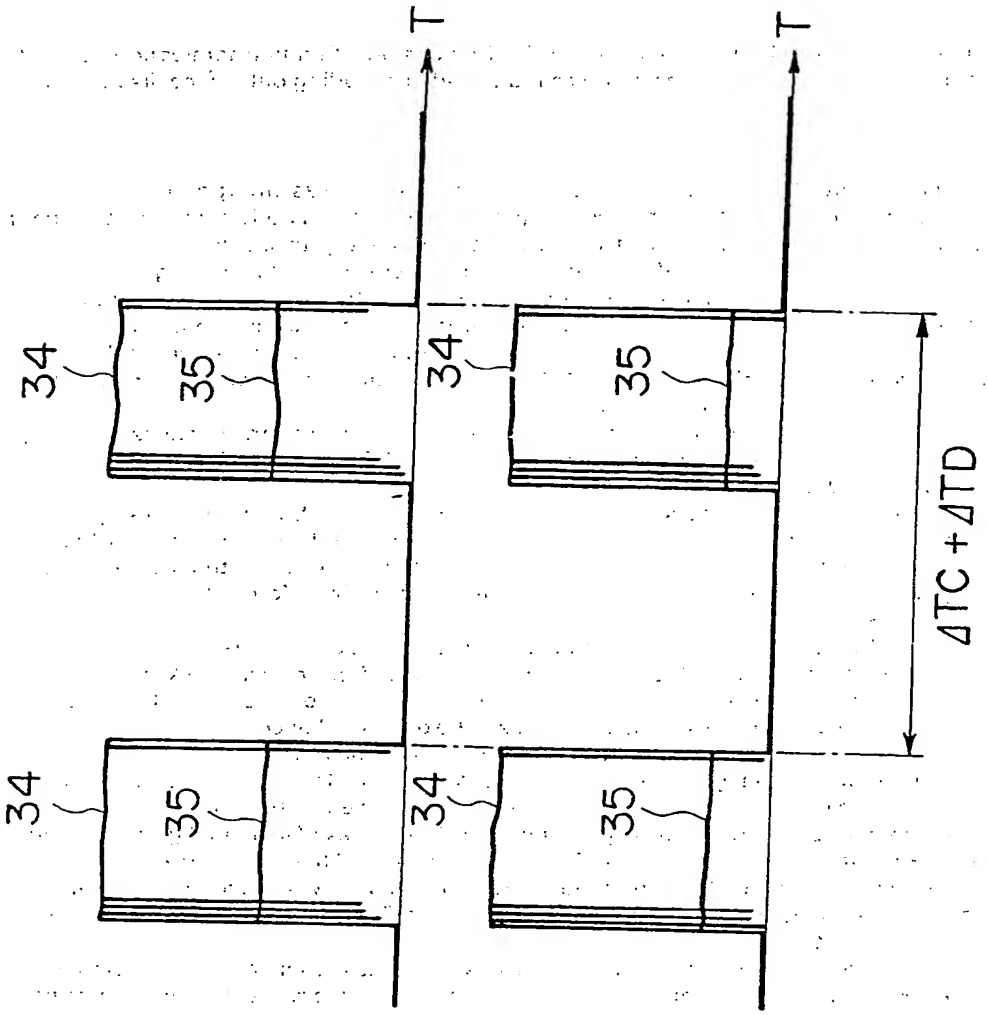


FIG. 18A

FIG. 18B

SPECIFICATION

Method for driving matrix circuit

Background of the invention

Field of the invention

The present invention relates to a method for driving a matrix circuit using a thin-film semiconductor and more particularly it relates to a method for driving a matrix circuit used in a reading out device displaying device.

Description of the prior art

Recently, attention has been drawn to a thin-film semiconductor made of such as amorphous siliconhydride (a-Si:H) or cadmium sulfide-cadmium selenide (CdS-Cdse) sintered body, which is utilized for such as a large scale image sensor for a facsimile or a two dimensional liquid crystal display.

A thin-film semiconductor is readily deposited, if desired, on a transparent substrate by using a glow discharge method, reactive sputtering method, vapor deposition method or the like. Further, the thin-film semiconductor is fabricated, by using a general photolithography process, into an array composed of photodiodes, photoconductive photosensors, field effect transistors or the like. Thus, it features in that inexpensive large scale and large area reading out and displaying devices can be fabricated which have been impossible to realize with conventional crystalline semiconductors.

In order to simplify the circuit and to make available of a two dimensional use, a matrix circuit is generally used for a reading out or displaying device. Therefore, a matrix circuit used, for example, in a large scale image sensor will now be described hereinafter.

Figures 1 and 2 show matrix circuits for a large scale image sensor. Referring to both figures, a single block is made of n (in the figures $n=4$) unit elements e of a thin-film semiconductor, and an array is made of m blocks. For the purpose of illustration, the unit element is denoted as e_{ij}, the suffix i being the block number and the suffix j being the position number of the unit element within its block. Therefore, it follows $1 \leqq i \leqq m$, $1 \leqq j \leqq n$.

In Figure 1, the unit elements for each block are connected in common at the side of one terminal of each unit element, and the unit elements (e_{i1} to e_{i4} : $1 \leqq i \leqq 4$) having the identical suffix j in each block are respectively connected at the side of the other terminal of each unit element to lines l_1 to l_4. The lines l_1 to l_4 are connected to respective switches 1 to 4 of a switch array so as to be grounded or connected to corresponding input terminals of an amplifier 5 under operations of the switches 1 to 4.

Each unit element e_{ij} is applied with a voltage V_j (i represent a block number ; $1 \leqq i \leqq m$) independently for each block. The unit elements e_{i1} to e_{i4} are enabled while the voltage V_j is applied. In this case, since an image sensor is exemplarily employed, currents corresponding to the intensities of incident lights flow and are sequentially input to the amplifier 5 under operation of the switch array, and the input currents are amplified. Also, since the voltages V_1 through Vm are sequentially applied as shown in a timing chart of Figures 3, each current corresponding to the intensity of incident light and flowing through each one of the unit elements e is sequentially input to the amplifier 5.

In contrast with the above, the matrix circuit shown in Figure 2 has lines l_1 to l_4 connected to respective input terminals of amplifiers 6 through 9 whose output terminals are connected to respective input terminals of allocated regions of a shift register 10. The shift register 10 sequentially outputs the stored contents as a time series signal every time a not shown shift pulse is input thereto. The voltages V_1 through Vm are applied in the manner as shown in Figure 3. Thus, in the matrix circuit of Figure 2, similar to the matrix circuit of Figure 1 currents corresponding to the intensities of incident lights for every unit elements e in the array can sequentially be obtained.

It is here to be noted that in order to make the operation of the unit elements e_{ij} in the whole array finish within Ta seconds, each unit element e_{ij} must theoretically be in a normal operation condition within not so later than Ta/m seconds after application of the voltage Vi. For instance, if Ta = 10 msec and m = 64, then Ta/m = 156 μsec. Although there is 156 μsec margin according to calculation, it is, in practice, not possible to obtain the margin more than about 50 μsec due to various restrictions.

Figure 4A through Figure 4C are graphs showing a change of current relative to a lapsed time after application of a voltage of 10 V to a unit element e_{ij} which in this case is a coplaner type photoconductive photosensor with a gap length of 10 μ m and ohmic contacts for electrodes obtained on an n⁺ layer. The abscissa represents a time (μsec), and the ordinate represents a current (A).

Figure 4A stands for a case with an illuminance of 100 (*lx*), Figure 4B stands for a case with 10 (*lx*), and Figure 4C stands for a dark case, respectively.

As is apparent from the graphs, a large current flows immediately after the voltage of 10 V is applied, however, a lapse of about 200 μsec makes the current enter in a ordinary state. It is noticed that the current immediately after application of the voltage is remarkably large as compared with a current under an ordinary state, particularly in the 10 (*lx*) and dark cases, respectively of Figure 4B and Figure 4C. The current in the 100 (*lx*) case in an ordinary state is about five times as large as that in the 10 (*lx*) case, while on the other hand at the time immediately after application of the voltage, it is about two or three times. Thus, it is understood that the discrimination between the light intensities is hard to obtain. That is, with a conventional

type image sensor, an erroneous operation is likely to occur in reading out an original.

The methods of solving such problems may be thought of such as prolong the time *Ta* for the whole array unit elements e_{ij} or to increase the number *n* of unit elements in a block, in the latter case the number of the switches 1 to 4 are increased as for Figure 1 and the number of the amplifiers 6 to 9 are increased as for Figure 2.

These methods, however, degrade the properties of the device and in addition a rise of cost is brought about so that such methods for solving the problems are not practicable.

Summary of the invention

The present invention has been made in view of the above prior art problems, and it is an object of the present invention to provide a method for driving a matrix circuit which is free from an erroneous operation and a high speed operation together with a low cost can be attained.

The above object can be attained by practicing the following method according to the present invention: a method for driving a matrix circuit including a plurality of blocks, each block having a plurality of thin-film semiconductor unit elements connected so as to be simultaneously applied with a voltage which enables the unit elements, in which the plurality of blocks are sequentially applied with a voltage to make the plurality of unit elements for respective blocks sequentially enabled, characterized by applying a voltage *Vz* to any desired one of the plurality of blocks, during a period which is before the time duration while the one block is applied with a voltage *Vx* for making the one block enabled and which is during the time duration while no other blocks other than the one block are applied with a voltages *Vy* for making the other blocks enabled.

Brief description of the drawings

Figure 1 is a schematic circuit diagram showing a first example of a matrix circuit;
Figure 2 is a schematic circuit diagram showing a second example of a matrix circuit;
Figure 3 is a timing chart showing timings of applied voltages V_1 to *Vm*,
Figure 4 shows time characteristics of photocurrents of a thin-film semiconductor, wherein
Figure 4A shows a characteristic curve in a 100 (*lx*) case,
Figure 4B shows a characteristic curve in a 10 (*lx*) case, and Figure 4C
Figure 4C shows a characteristic curve in a dark case;
Figure 5 shows frequency characteristic curves of photocurrents of a thin-film semiconductor;
Figure 6A is a diagrammatical view showing an initial state of a semiconductor when a voltage is applied thereto;
Figure 6B is a diagrammatical view showing the ordinary state of the semiconductor;
Figure 7 is a timing chart of applied voltages *Vi* for illustrating an embodiment according to the present invention;
Figure 8 is a characteristic curve showing a change of light intensity dependence by using as stet duty ratios of repetitive pulses;
Figure 9 is a partial circuit diagram of the matrix circuit of Figure 2 to which a diode is added;
Figure 10 is a voltage-current characteristic curve of a diode shown in Figure 9;
Figure 11 shows characteristic curves illustrating a relation between the number of pulses and photocurrent in a thin-film semiconductor;
Figure 12 is a circuit diagram showing a more detailed arrangement of the matrix circuit shown in Figure 1;
Figure 13 is a waveform diagram of the pulse signal S_1 in Figure 12;
Figure 14A is a waveform diagram of a pulse signal S_1;
Figure 14B is a waveform diagram of a pulse signal S_2 relative to the timings of the pulse signal S_1;
Figure 15A is an output signal waveform diagram obtained with a prior art matrix driving method using the matrix circuit of Figure 12;
Figure 15B is an output signal waveform diagram obtained with a driving method according to the present invention;
Figure 16 is a more detailed circuit diagram of the matrix circuit of Figure 12 in which diodes are added;
Figures 17A, 17B and *17C* show waveforms of pulse signals S_1, S_3, and S_4, respectively;
Figure 18A is an output signal waveform diagram obtained with a prior art matrix driving method using the matrix circuit of Figure 16; and
Figure 18B is an output signal waveform diagram obtained with a driving method according to the present invention.

Detailed description of the preferred embodiment

Prior to proceeding to the description of the embodiments according to the present invention, the theoretical basis how the method for driving a matrix circuit according to the present invention is practiced is first described.

Figure 5 is a graph made up by measuring dependence of a current Ip upon a pulse frequency of a pulse voltage applied to a unit element of a thin-film semiconductor (in this case, the voltage is 10 V and the pulse duty ratio is 50%), the current being that at the time instant after 50μsec from the rise time of the pulse voltage. The curve 11 stands for an illuminance of 100 (lx), and the curve 12 stands for an illuminance of 10 (lx).

As can be seen from the graph, in both 100 (lx) and 10 (lx) cases, the current Ip tends to decrease as the frequency of repetitive pulses goes higher, and particularly in the 10 (lx) case, the decrease is remarkable. Therefore, in a higher frequency range, the current in the 100 (lx) case reaches about 4.3 times as large as that in the 10 (lx) case, which comes near at the ordinary state (about 5 times). This phenomenon is theoretically discussed below.

Upon application of a high electrical field through electrodes, to a semiconductor having a relatively high resistivity carriers (for instance, electrons) are generally injected through the electrode, and a space charge is formed within the semiconductor. The current flowing through the semiconductor is determined by this space charge, and such a current is called a space charge limited current (hereinafter abbreviated as SCLC). In an ordinary state, the magnitude I of SCLC is given by the following equation:

$$I = K V^2 \theta \mu / 4 \pi L^3 \times 10 \ [A/cm^2] \quad \ldots (1)$$

wherein K is a dielectric constant, V is an applied voltage, μ is a mobility of the semiconductor, L is a distance between the electrodes, and θ is a ratio (Nc/Nt) of a carrier density Nc in the conduction band of the semiconductor to the carrier density Nt at a trap level sufficiently shallow not to make the carrier in the conduction band become a combination center.

However, since the state immediately after the electrical field is applied to the semiconductor is not a one like an ordinary state, carriers injected through the electrode hardly fall into the trap level. Figure 6A schematically shows such an initial state.

In Figure 6A, a voltage has just been applied to opposite ends of a semiconductor 13, that is, to a plus electrode side 14 and a minus electrode side 15, and a number of holes 18 are generated at the plus electrode side 14. Although shallow trap levels 16 exist in the semiconductor 13, electrons injected from the minus electrode side 15 are still not made to fall into the shallow trap levels 16 at this stage of an initial state.

In this initial state, since Nc is sufficiently large as compared with Nt, the value of θ becomes large to thus make SCLC large as well.

As the time lapses, however, as some pairs of electrons 17 and the holes 18 disappear due to combinations therebetween and as a supply from the electrodes comes to an equilibrium condition, then it occurs that electrons 17 fall into the shallow trap levels 16 (indicated at 19) or electrons 17 are excited from the shallow trap levels 16 again up to the conduction band. As a result, the electron density comes to an equilibrium condition between the conduction band and the trap level 16. For this reason, the value of θ becomes nearly a constant value smaller than that at the initial state, and correspondingly SCLC also becomes smaller than that at the initial state and becomes nearly a constant value. From the above understanding, the phenomenon illustrated in Figure 4 may be clarified to some extent, in which all of the graphs show that current values are large at the initial state and thereafter come to be at a constant value.

In the cases of Figure 4A and Figure 4B, that is, in the cases where light is illuminated upon a semiconductor, although circumstances become more complicated, the current can be expressed nearly by the following equation;

$$I = q \mu N c(F) V / L + K V^2 \theta \mu / 4 \pi L^3 \quad \ldots (2)$$

wherein q is an electric charge, Nc(F) is an electron density in the conduction band under an incident light intensity F and without application of electrical field.

The first term in the equation (2) represents a current changing depending upon the incidence light intensity F, and the second term represents SCLC. In other words, the difference between the current values at the ordinary state of Figures 4A and 4B is depending upon the difference of the current in the first term.

In the initial state immediately after the voltage is applied, the value of the second term becomes large as discussed previously, so the difference of current values is hard to be depending upon the difference of incident light intensities F. In other words, it can be considered that the dependence of current upon the light intensity becomes small immediately after application of the voltage. This, as a result, caused an erroneous operation of the prior art image sensor or the like.

Alternatively, another phenomenon appears as shown in Figure 5 in which under application of a repetitive pulse voltage, the current Ip at the time of 50 μsec after the voltage application decreases depending upon the pulse frequency, and particularly in a relatively high frequency range, the light intensity dependence of the current Ip becomes strong. Such phenomenon can be understood pursuant to the way of the above analysis as follows.

That is, if a relatively high frequency repetitive pulse voltage is applied, electrons are likely to always exist at a shallow trap level because the electrons cannot get out of the shallow trap level. Therefore, since θ in the second term of the equation (2) does not become sufficiently large at the initial state, the current Ip decrease proportionately and the current in the first term is greatly depending upon the current Ip. That is, the

difference of the light intensities F is sufficiently depending upon the current Ip.

The features of transient response of the current as described above is considered as distinguished in a thin-film semiconductor which is known as having a number of shallow trap levels.

A further description of the matrix circuits shown in Figures 1 and 2 is made in view of the experimental results and its theoretical analyses described above.

In the matrix circuits shown in Figures 1 and 2, the voltage Vi is applied to each block at the timings shown in Figure 3. In the timing chart of Figure 3, it is possible to set a time duration between the periods while each block is made enabled under application of the voltage Vi, during the time duration, none of the blocks being made enabled. Thus, if a voltage is applied to all of the blocks during the thus set time duration, it has the same effect for any one of the selected blocks that as if a pulse voltage with a certain frequency has been applied before the one block becomes enabled. The timings of the voltages Vi is shown in Figure 7.

Figure 7 shows a timing chart of applied voltage Vi ($1 \leqq i \leqq 5$) in the matrix circuits with the number of blocks set as $m = 5$ in Figures 1 and 2 and shows a first embodiment of the matrix circuit driving method according to the present invention.

As one example, here the voltage V_4 is taken into consideration. Before the time duration T_4 while the fourth block is in an enabled state, a repetitive pulse voltage is applied. This can be accomplished by applying voltages V_1 through V_5 during the time durations P_1 through P_4 other than the time durations T_1 through T_3 while the first through third blocks come into an enabled state. This circumstance can be applied similarly not only to the fourth block but also to all other blocks.

By applying the voltage Vi of this nature, as previously described, light intensity dependence of photocurrent of the unit element e_{ij} is enhanced.

In a practical operation, it is desirable that the larger the ratio $Ti/(Ti + Pi)$ relating to the time duration in an enabled state of each block is. In other words, it is preferable that the smaller the duty of the repetitive pulse is. The maximum value of the duty ratio is $Pi/(Ti - Pi)$. As can be seen from Figure 8, the light intensity dependence of the current Ip is not so degraded even if the duty ratio is made small. Therefore, it is possible to improve the characteristics without in the least decreasing the ratio of the enabled durations. In the graph shown in Figure 8, the abscissa represents the duty ratio of the repetitive pulse, and the ordinate represents a ratio $Ip(100)/Ip(10)$ of the current $Ip(100)$ at $100(lx)$ to the current $Ip(10)$ at $10(lx)$.

Next, some problems and the method of solving them are described, which problems are brought into existence while the timing chart of Figure 7 according to the present invention is applied to Figures 1 and 2.

If all the voltages are applied to the blocks at a timing shown in Figure 7, the large currents flow on the lines l_1 to l_4 during the time duration Pi. As the currents are supplied to the amplifiers 5 or 6 to 9, there is a possibility that the currents are in axcess of the dynamic ranges of the amplifiers, resulting in adversely influence of the characteristic of the amplifiers. In order to solve this problem, the switches 1 to 4 in the matrix circuit of Figure 1 may be operated in such a manner that the lines l_1 to l_4 are all grounded during the time duration Pi while all of the blocks are applied with the voltages.

Alternatively, in the matrix circuit of Figure 2, the problem may be solved by providing by-pass circuits at the pre-stage of the amplifiers 6 to 9.

Figure 9 shows one examples of a by-pass circuit for a large current passing on the line l_1 in which a Schottky diode 20 is connected at the pre-stage of the amplifier 6 in Figure 2 The other amplifiers 7, 8 and 9 are also provided with such by-pass circuits. The Schottky diode 20 has, as shown in Figure 10, V-I characteristics that the current I does no flow at all within a low voltage v range even in a forward direction, and that the resistivity abruptly becomes small and a large current I flows within a relatively high voltage v range. By utilizing these characteristics, even if a large current flows, for example, on a line l_1 (the same is also true for the other lines l_2 to l_4) and the amplifier 6 becomes saturated, the input voltage rise at the amplifier 6 can be avoided because in such a case the resistivity of the Schottky diode 20 becomes small. On the contrary, if a certain block comes into an enabled state and a smaller current flows on the line l_1, the Schottky diode 20 comes into a high resistivity state since the input voltage at the amplifier is sufficiently small and the current per se on the line I is directly input to the amplifier 6.

The first embodiment of the present invention has been described above in which the voltage Vi is applied at the timing shown in Figure 7. It is not necessarily required to always apply the repetitive voltage to all of the blocks. It has been known that an enough effect can be obtained by applying a suitable number k of voltage pulses to a block before the block becomes enabled.

Figure 11 is a graph showing a relation between the number k of pulses and the current Ip, wherein the abscissa represents the number k of pulses and the ordinate represents the current Ip. The curve 21 stands for the case at 100 (lx) and the curve 22 stands for the case at 10 (lx). As shown in the graph, regardless of the fact that whether the number k of pulses having been applied previously is 10 or 5, the ratio $Ip(100)/Ip(10)$ of the current $Ip(100)$ at $100(lx)$ to the current $Ip(10)$ at 10 (lx) takes a sufficiently large value.

Examples of the matrix circuits shown schematically in Figures 1 and 2 are explained, and by using the examples, a further description of the first embodiment of the matrix circuit drive method shown in Figure 7 according to the present invention will be done in detail.

A circuit diagram shown in Figure 12 is a version of the matrix circuit shown in Figure 1. The circuit of Figure 12 differs in that a single block is made of 32 unit elements e_{ij} of a thin-film semiconductor, and a matrix section 23 is made of 64 such blocks. Therefore, in this case, $m = 64$ and $n = 32$.

The matrix section 23 may be fabricated by using the following steps. First, after a washed glass substrate (manufactured by Corning Co., 7059 glass) is mounted on an anode within a glow discharge device, the device was set at vacuum of 10^{-6} Torr. Next, high purity monosilane gas (SiH_4) and 10 ppm phosphine gas (PH_3) diluted in high purity hydrogen gas (H_2) were flowed into the glow discharge device, respectively at the flow rate of 10 SCCM (standard cc/min) and 5 SCCM. At that time, the pressure within the device was maintained at 0.1 Torr. Thereafter, a glow discharge was generated between parallel plate type electrodes under a high frequency of 1356 MHz, and an a-Si layer of about 7000Å was deposited upon the glass substrate. At that time, the glass substrate was maintained at 200 °C. Succeedingly, SiH_4 at the flow rate of 2 SCCM and 1000 ppm PH_3 gas diluted in high purity hydrogen gas (H_2) at the flow rate of 10 SCCM were flowed into the device. And similarly to the above, a glow discharge was generated to deposite a low resistivity n^+ layer of about 1000 Å upon a-Si layer.

Further, after Al of about 2000 Å is vapor deposited upon the n^+ layer, the Al vapor deposited layer was selectively removed leaving the portions where electrodes and lower layer wirings are formed, by using a known photolithography technique.

Then an exposed n^+ layer was removed by means of a dry etching method using the Al pattern as a mask. Thus, the manufacturing of the unit element e_{ij} was completed.

Next, the process for wirings the unit elements e_{ij} is performed. First, after application of a polyimide resin (a trade name PIQ = polyimide isoindolc quinazolinc dione) and baking, contact holes for conduction to upper layer wirings were formed at a photolithography process. The upper layer wirings were formed at a further photolithography process after Al of about 500 Å is vapor deposited.

The matrix section 23 formed in the above process is connected to a common electrode side drive section 24 (hereinafter referred to as common section 24) applying an application voltage V*i*, and to a separate electrode side drive section (hereinafter referred to as separate electrode section 25) outputting time series signals by transforming input photocurrents from the unit element e_{ij}, respectively.

The common section 24 is arranged as in the following. The parallel output terminals of a shift register 26 (64 bit arrangement) are respectively connected to the input terminals of inverters IN*i* ($1 \leqq i \leqq 64$, which is applicable to all suffixes used in this embodiment) and the gate electrodes of transistors TRi_1. The output terminals of the inverters IN*i* are connected to the gate electrodes of transistors TRi_0. The plus terminal of a DC power source 27 is connected to the source terminals (or drain terminals) of the transistros TRi_1, while the minus terminal is grounded and also connected to the drain terminals (or source terminals) of the transistors TRi_0. Connected to a common terminal of the unit elements e_{ij} of the matrix section 23 are the drain terminals (or source terminals) of the transistros TRi_1 and the source terminals (or drain terminals) of the transistors TRi_0, thereby applying the application voltage V*i* to the matrix section 23.

Next, the arrangement of the separate section 25 is described. The source terminals (or drain terminals) of transistros $TRAj_0$ ($1 \leqq j \leqq 32$, which is applicable to all suffixes in this embodiment) are connected to respective lines l_j of the matrix section 23 and source terminals (or drain terminals) of transistors $TRAj_1$ as well. The parallel output terminals of a shift register 28 (here it is of a 32 bit arrangement) are connected to the input terminals of inverters IN*j* and the gate electrodes of the transistors $TRAj_1$ as well. The drain terminals (or source terminals) of the transistors $TRAj_1$ are connected to the input terminal of an amplifier 29, and the drain terminals (or source terminals) of the transistors $TRAj_0$ are grounded.

The operation of the matrix circuit activated by the drive method according to the present invention will now be described.

First, in order to apply the voltage V*i* with the timing shown in Figure 7, a pulse signal S*i* shown in Figure 13 is input to the shift register 26 to thereby sequentially shift the register 26 with a shift pulse of 50 KHz.

In this embodiment, the pulse period T*a* of the pulse signal S*i* is 5.12 msec, the pulse width Δp of the repetitive pulse is 20 μsec, and the time duration between the repetitive pulses or time duration ΔT during which a block is enabled is 60 μsec.

In the first block (suffix $i = 1$) in Figure 12, for instance, if the content of R_1 of the shift register 26 is of a high level, the transistor TR_{11} turns ON so that the voltage V of the DC power source 27 is applied to the first block as an applied voltage V*i*. If the contents of the R_1 goes to a low level, then the transistor TR_{11} turns OFF so that in contrast with the above, a high level voltage is applied through the inverter IN_1 to the gate electrode of the transistor TR_{10}. Therefore, the transistor TR_{10} turns ON to make the common terminal of the first block grounded, which results in the voltage $V_1 - 0$. Thus, while the pulse signal S_1 shown in Figure 13 passes through the R_1 of the shift register 26, the voltage V_1 changing in response to the same timing can be obtained. The operations of the voltages V_2 to V_{64} of the other blocks are identical to the above operation except the time delay therebetween. Therefore, with the pulse signal S_1, the voltages V*i* with the timing shown in Figure 7 can be obtained.

The separate section 25 functions to sequentially deliver photocurrents of the unit elements e_{i1} to e_{i32} to the amplifier 29 during the time period from the time the voltage V*i* is applied to the time the voltage V*i* becomes zero.

To this end, a pulse signal S_2 shown in Figure 14B is input to the shift register 28 to make the register shift by a shift pulse of 1 MHz. The pulse signal S_1 is shown in Figure 14A for reference.

In the embodiment, the time duration $\Delta P - TA$ from the time instant when a pulse of the pulse signal S_1 rises to the time instant when a pulse of the pulse signal S_2 rises is 20 μsec − 28 μsec = 48 μ sec, and the pulse width ΔPe of the pulse signal S_2 is 1 μsec. Therefore, the time duration ΔTB for shifting the shift register 28 from SR_1 to SR_{32} μ sec.

It is assumed here that the unit elements e_{i1} to e_{i32} are applied with the voltage V*i* during the time duration ΔT of the pulse signal S_1 shown in Figure 14 A. At the time instant when $\Delta TA = 28$ μsec is lapsed after the start of the time duration ΔT, the SR_1 of the shift register 28 is supplied with the pulse S_2 and the contents thereof goes to a high level. As a result, the transistor TRA_{11} turns ON, and the photocurrent flowing through the unit element e_{i1} is input to the amplifier 29. Succeedingly, the high level sequentially shifts from the SR_2 to SR_{32} with the help of the shift pulse of 1 MHz, and accordingly the photocurrents of the unit elements e_{i2} to e_{i32} are sequentially input to the amplifier 29 to thereby obtain the time series signal S_0. In this case, while the voltage V*i* remains in the time duration ΔP of the repetitive pulse, the contents of the shift register 28 are all in a low level. Therefore, a high level is applied through the inverter INV*j* to the gate electrode of the transistor $TRAj_0$ so that the transistor $TRAj_0$ turns ON to ground the line *lj*.

Figure 15A is a view of an output waveform the amplifier 29 where the prior art voltage pulse shown in Figure 3 is applied to the matrix circuit shown in Figure 12, while Figure 15B is a view of an output waveform from the amplifier 29 in the embodiment according to the present invention. The curve 30 stands for a 100 (*lx*) case, and the curve 31 stands for a 10 (*lx*) case.

In Figure 15A where a uniform illumination was employed, there is a difference between the output signal amplitudes of the first and last unit elements within a single block. In addition, the ratio of the output signal amplitude for the 100 (*lx*) case to that for the 10 (*lx*) case is relatively small. On the contrary, in Figure 15B, a notable improvement is recognized.

Figure 16 is a circuit diagram of the matrix circuit of Figure 2. In Figure 16, a matrix section 23 and a common section 24 are identical to the circuit shown in Figure 12, and a pulse signal S input to a shift register is also identical to that described with Figure 12. Therefore, the description therefor is omitted except for a separate section 25.

One terminal of a Schottky diode D*j* ($1 \leq j \leqq 32$, which is applied to all of the suffixes in the present embodiment) is connected to the line *lj* in a manner that the diode is forward-biased while the line *lj* is at a higher potential. The other terminal is grounded. The line *ij* is connected to the input terminal of the amplifier AMP*j* whose output terminal is connected to the parallel input terminal of a shift register 33 through a sample hold circuit 32.

Figure 17A shows the pulse signal S_1 input to the shift register 26. It is assumed that the voltage V*i* for enabling the unit elements e_{i1} to e_{i32} during the time duration ΔT of the pulse signal S_1 is applied. In this case, photocurrents flowing through the unit elements e_{i1} to e_{i32} are amplified by the amplifiers AMP_1 to AMP_{32} and in turn input to the sample hold circuit 32. The sample hold circuit 32 does not hold the signals form the AMP*j* unless it receives a hold signal S_3 shown in Figure 17B.

As shown in Figure 17B, the hold signal S_3 is input to the sample hold circuit 32 at the end of the time duration ΔT, whereby the output from the amplifiers AMP_1 to AMP_{32} at that time are held by the sample hold circuit 32 and stored in the shift register 33. Thereafter, a shift pulse of 1 MHz shown in Figure 17C is input to the shift register 33 during the time duration $\Delta TC - 32$ μsec, and the stored content stet output as a time series signal S_0 from the serial output terminal.

Figure 18A shows a waveform of the time series signal S_0 while the voltage V*i* with the timing shown in Figure 3 is applied, and Figure 18 shows a waveform of the time series signal S_0 while using the drive method according to the present invention. The curve 34 stands for the 100 (*lx*) case, while the curve 35 stands for the 10 (*lx*) case.

In the matrix circuit shown in Figure 16, since the signal is sampled by the sample hold circuit at the end of the time duration ΔT during which the unit element e_{ij} are enabled, each unit element is in a stable state and therefore there is no difference between the output values output at different times. However, the output signal ratio of the 100 (*lx*) case to the 10 (*lx*) case still remains small. On the contrary, by using the drive method according to the present invention, a notable improvement is recognized as shown in Figure 18B.

The above description has been made with reference to a large scale image sensor, however, it is not limited thereto, but the drive method according to the present invention may also be applied to drive other thin-film semiconductor devices. For example, the present method may be applied to a TFT (Thin-Film Transistor) two dimensional device used for such as an LCD (Liquid Crystal Display), ECD (Electrochromic Display) or the like.

As described in detail heretofore, the matrix circuit drive method according to the present invention can enjoy a remarkable effect that a maxtrix circuit can be realized in which an erroneous operation is not likely to be occurred and a manufacturing cost is small while the operational efficiency of the unit element is improved.

CLAIMS

1. A method for driving a matrix circuit including a plurality of blocks, each block having a plurality of thin-film semiconductor unit elements connected so as to be simultaneously applied with a voltage which enables the unit elements, in which the plurality of blocks are sequentially applied with a voltage to make the plurality of unit elements for respective blocks sequentially enabled, characterized by applying a voltage *Vz* to any desired one of said plurality of blocks, during a period which is before the time duration while said one block is applied with a voltage *Vx* for making said one block enabled and which is during the time duration while no other blocks other than said one block are applied with a voltage *Vy* for making said other blocks enabled.

2. A method according to Claim 1, wherein the application of said voltage *Vz* is repeated while said matrix circuit is being operative.

3. A method according to Claim 1, wherein said voltage *Vz* is repeatedly applied to all of said blocks while said matrix circuit is being operative.

4. A method according to Claim 1, wherein the thin-film semiconductor for said unit elements is made of amorphous silicon hydride.

5. A method according to Claim 1, wherein the thin-film semiconductor for said unit elements has a photoconductivity.

6. A method according to Claim 1, wherein said unit elements are composed of photodiodes.

7. A method according to Claim 1, wherein said unit elements are composed of photoconductive photosensors.

8. A method according to Claim 1, wherein said unit elements are composed of field effect transistors.

9. A matrix driving circuit having means for applying to elements thereof a predetermined voltage separate from a voltage which enables said elements.

10. A circuit substantially as herein described with reference to any of the accompanying drawings.

11. A method of driving a matrix substantially as herein described with reference to any of the accompanying drawings.

Printed in the UK for HMSO, D8818935, 6 85. 7102.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.